REMARKS

Applicants thank Examiner for acknowledging receipt of foreign priority document, Japanese Application No. JP10-337764, that has been submitted pursuant to 35 U.S.C. § 119.

Applicants have amended the attached drawings for Figures 9 and 10 to include the designation of "Prior Art" as required by MPEP §608.02(g).

Applicants have also amended the Specification to correct the Figure number references in the "Background of the Invention." No new matter has been added.

Claims 1,2,5,6, and 8 have been amended to clarify the novelty of the invention being claimed. Claims 9-12 have been added in order to further specify the invention as disclosed in the specification.

As requested by Examiner, Applicants have attached a new Abstract that is 101 words in length.

As requested by Examiner, the Title has been amended to "SOLID-STATE IMAGE-PICKUP DEVICE HAVING AN ACCUMULATION GATE FOR READING-OUT, ACCUMULATING, AND ALLOCATING SIGNAL CHARGES."

Applicants respectfully request reconsideration of Examiner's rejection of claims 1 - 8 under 35 U.S.C §102(b). Applicants submit that the prior art references of record, whether considered alone or in combination fail to either teach or suggest Applicants' claimed invention.

In rejecting claim 1, Examiner asserts that *Elabd et al.* (U.S. Patent No. 5,196,939) teaches Applicant's invention in Column 1, lines 65-68; Column 2, lines 12-17; and Column

4, lines 28-41. Applicants submit that this characterization of the prior art is inaccurate and the rejection should be withdrawn.

Specifically, Applicants note that the *Elabd* patent is directed to achieving high-frame rate transfer of images by only transferring a desired portion of a captured image, and thereby decreasing the transfer time and increasing the charge efficiency. (Col. 1, lns 46-52). The only way *Elabd* purports to improve image quality, increase frame rate, and increase charge efficiency is by reducing the amount of data to transfer by only transferring a desired portion of the image. This decreases the data-transfer time, the amount of data needed to be transferred, and the hardware required to quickly transfer an entire image, thereby decreasing the amount of charge-leakage and maintaining a higher image quality and frame-rate. Nothing in *Elabd* teaches or suggests anything beyond Applicant Admitted prior art as far as the structure and timing of the image capture of the pixel charges is concerned.

Elabd teaches transferring each row of image data separately, and transferring even pixels separately from odd pixels, as disclosed in Applicant admitted prior art. (See Col. 4, lns 42-48) Applicants note that Examiner fails to point out anywhere that *Elabd* discloses technology relating to Applicant's simultaneous image capture technology. Examiner asserts in his rejection of Claim 1 that he views the storage register (33) in *Elabd* as the accumulation gate. However, the storage register in *Elabd* is used simply as temporary storage of row image data. Once a row of image data is loaded into the storage register (33), it is compared to see whether this is part of the image desired to be loaded. If it is not, that row is sent to the Dump Drain (35). If it is part of the image desired, it is transferred into

Transfer Registers A and B (17A and 17B) and sent to the output. There is but one storage register (33) in the device that holds only one row of image data at a time, and the register has nothing to do with the capture of the image data from the image sensors. Therefore, the storage register (33) is not an accumulation gate, as described in Applicant's disclosure. In conclusion, Applicants maintain that *Elabd* maintains the shortcomings of the prior art by maintaining spatial and time-based deviations in signal-charge fetching and differences in sensitivity caused by differences in read-out timing.

Applicant's invention, however, is directed to a solid-state image-pickup device which improves upon the prior art via the addition of an accumulation gate positioned between the sensor array and the transfer registers. The addition of this accumulation gate allows the device to capture the image data from every image sensor at the same time and store into the accumulation gate, and then (in one embodiment) afterwards transfer even and odd pixel data separately to respective transfer registers. Because the image data is entirely captured at the same time before beginning the process of transferring image data towards the output port, Applicants gain the advantage of eliminating variations in accumulation period from sensor to sensor, spatial and time deviations in signal charge, and differences in sensitivity caused by differences in read-out timing. At no point does *Elabd* teach or suggest this method or apparatus.

Examiner's remaining references cited but not relied upon, considered either alone or in combination, also fail to teach applicant's currently claimed invention. In light of the foregoing, Applicants respectfully submit that all claims now stand in condition for allowance.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail on December 24, 2003 in an envelope addressed to:

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